IN THE CLAIMS:

Please amend claims 1, 9, 14-21, and 35, and add new claims 36-39 as follows:

1. (Currently Amended) A method for forming a low resistivity titanium silicide layer on a surface of ~~a~~ at least one previously doped region of a silicon semiconductor substrate, said method comprising the steps of:

depositing a titanium layer on the surface of the doped region of the silicon semiconductor substrate, the doped region ~~being~~ having been previously doped to form an n-type or p-type source or drain region;

performing a rapid thermal annealing of the silicon semiconductor substrate coated with the titanium layer in order to form titanium silicide; and

before the step of performing the rapid thermal annealing, introducing an effective amount of a metallic element at least at the interface between the titanium layer and the doped region of the silicon semiconductor substrate, the metallic element being chosen from the group consisting of indium, gallium, tin, and lead,

wherein the rapid thermal annealing step anneals the titanium layer with the introduced metallic element so that the introduced metallic element ~~so as to promote~~ promotes titanium silicide transformation from C49 phase to C54 phase during ~~a subsequent~~ the rapid thermal annealing~~, the metallic element being chosen from the group consisting of indium, gallium, tin, and lead; and~~

~~after the introducing step, performing a rapid thermal annealing of the silicon semiconductor substrate to form titanium silicide~~.

2. (Original) The method as defined in claim 1, wherein the metallic element is chosen from the group consisting of indium and gallium.

3. (Original) The method as defined in claim 1, wherein the metallic element is indium.

4. (Original) The method as defined in claim 1, wherein the effective amount of the metallic element is 1×10^{13} to 5×10^{14} atoms/cm^2.

5. (Original) The method as defined in claim 1, wherein the effective amount of the metallic element is 5×10^{13} to 5×10^{14} atoms/cm^2.

6. (Original) The method as defined in claim 1, wherein the effective amount of the metallic element is 5×10^{13} to 3×10^{14} atoms/cm^2.

7. (Previously Presented) The method as defined in claim 1, wherein the introducing step includes the sub-step of depositing the effective amount of the metallic element on the surface of the doped region of the silicon semiconductor substrate.

8. (Previously Presented) The method as defined in claim 1, wherein the introducing step includes the sub-step of implanting the effective amount of the metallic element into the doped region of the silicon semiconductor substrate.

9. (Currently Amended) The method as defined in claim 8,
wherein the implanting sub-step is performed before the depositing step, and
the implanted metallic element is not thermally annealed before the depositing step.

10. (Original) The method as defined in claim 8, wherein in the implanting sub-step, the metallic element is implanted into the silicon semiconductor substrate to a depth of 5 to 25 nm.

11. (Original) The method as defined in claim 8, wherein in the implanting sub-step, the metallic element is implanted into the silicon semiconductor substrate to a depth of 8 to 20 nm.

12. (Original) The method as defined in claim 8, wherein in the implanting sub-step, the implantation energy is 5 to 30 keV.

13. (Original) The method as defined in claim 8, wherein in the implanting sub-step, the implantation energy is approximately 25 keV.

14. (Currently Amended) The method as defined in claim 1,

wherein the introducing step is performed before the depositing step, and

the introduced metallic element is not thermally annealed before the depositing step.

15. (Currently Amended) A method for fabricating a semiconductor device, said method comprising the steps of:

doping at least one region of a silicon semiconductor substrate with a first metallic element to form an n-type or p-type source or drain region; and

after the doping step, forming a low resistivity titanium silicide layer on the surface of the at least one doped region of the silicon semiconductor substrate,

the forming step including the sub-steps of:

depositing a titanium layer on the surface of the at least one ~~n-type or p-type~~ doped region of ~~a~~ the silicon semiconductor substrate;

performing a rapid thermal annealing of the silicon semiconductor substrate coated with the titanium layer in order to form titanium silicide; and

before the sub-step of performing the rapid thermal annealing, introducing an effective amount of a second metallic element at least at the interface between the titanium layer and the at least one doped region of the silicon semiconductor substrate, the second metallic element being chosen from the group consisting of indium, gallium, tin, and lead,

wherein the rapid thermal annealing sub-step anneals the titanium layer with the second metallic element so that the second metallic element ~~so as to promote~~ promotes titanium silicide transformation from C49 phase to C54 phase during ~~a subsequent~~ the rapid thermal annealing~~, the metallic element being chosen from the group consisting of indium, gallium, tin, and lead; and~~

~~after the introducing step, performing a rapid thermal annealing of the silicon semiconductor substrate to form a low resistivity titanium silicide layer~~.

16. (Currently Amended) The method as defined in claim 15, wherein the second metallic element is chosen from the group consisting of indium and gallium.

17. (Currently Amended) The method as defined in claim 15, wherein the effective amount of the second metallic element is 1×10^{13} to 5×10^{14} atoms/cm^2.

18. (Currently Amended) The method as defined in claim 15, wherein the introducing ~~step includes the~~ sub-step ~~of~~ includes depositing the effective amount of the second metallic element on the surface of the at least one doped region of the silicon semiconductor substrate.

19. (Currently Amended) The method as defined in claim 15, wherein the introducing ~~step includes the~~ sub-step ~~of~~ includes implanting the effective amount of the second metallic element into the at least one doped region of the silicon semiconductor substrate.

20. (Currently Amended) The method as defined in claim 19, wherein in the implanting of the introducing sub-step, the second metallic element is implanted into the silicon semiconductor substrate to a depth of 5 to 25 nm.

21. (Currently Amended) The method as defined in claim 19, wherein in the implanting of the introducing sub-step, the implantation energy is 5 to 30 keV.

22-29. (Canceled)

30. (Previously Presented) The method as defined in claim 1, wherein the doped region is an n-type region.

31. (Previously Presented) The method as defined in claim 1, wherein the doped region is doped with arsenic.

32. (Previously Presented) The method as defined in claim 1, wherein the metallic element is chosen from the group consisting of gallium, tin, and lead.

33. (Previously Presented) The method as defined in claim 15, wherein the at least one doped region includes at least one n-type source or drain region.

34. (Previously Presented) The method as defined in claim 15, wherein the at least one doped region includes at least one region doped with arsenic.

35. (Currently Amended) A method for forming a low resistivity titanium silicide layer on a surface of a silicon semiconductor substrate, said method comprising the steps of:

depositing a titanium layer on the surface of the silicon semiconductor substrate;

introducing an effective amount of a metallic element at least at the interface between the titanium layer and the silicon semiconductor substrate ~~so as to promote titanium silicide transformation from C49 phase to C54 phase during a subsequent rapid thermal annealing~~, the metallic element being chosen from the group consisting of indium, gallium, tin, and lead; and

after the depositing and introducing ~~step~~ steps, performing a single rapid thermal annealing of the silicon semiconductor substrate coated with the deposited titanium layer so as to form C54 phase titanium silicide from the deposited titanium layer,

wherein the single rapid thermal annealing anneals the titanium layer with the introduced metallic element so that the introduced metallic element ~~promoting~~ promotes titanium silicide transformation from C49 phase to C54 phase during the single rapid thermal annealing.

36. (New) The method as defined in claim 8,

wherein the implanting sub-step is performed after the depositing step, and

the deposited titanium layer is not thermally annealed before the implanting sub-step.

37. (New) The method as defined in claim 19,

wherein the implanting of the introducing sub-step is performed after the depositing sub-step, and

the deposited titanium layer is not thermally annealed before the introducing sub-step.

38. (New) The method as defined in claim 19,

wherein the implanting of the introducing sub-step is performed before the depositing sub-step, and

the second metallic element is not thermally annealed before the depositing sub-step.

39. (New) The method as defined in claim 15, wherein the second metallic element that promotes titanium silicide transformation from C49 phase to C54 phase during the rapid thermal annealing is different than the first metallic element used in the doping step to form the n-type or p-type source or drain region.